

What is claimed is:

1. A semiconductor memory device that differentially amplifies data readout from a memory cell with reference to a reference value when data is read out, the semiconductor memory device  
5 comprising:
  - a reference cell; and
  - a load adjustor section that adjusts a first load connected to the reference cell in accordance with a selected address of the memory cell;
- 10 wherein the first load is adjusted with reference to a second load on a data path of the memory cell selected in accordance with the selected address.
2. A semiconductor memory device according to claim 1, wherein  
15 the second load is a load at a source terminal side of the memory cell according to the selected address, and the load adjustor section is arranged at a source terminal side of the reference cell.
- 20 3. A semiconductor memory device according to claim 1, wherein the first load is equivalent to the second load.
4. A semiconductor memory device according to claim 1, wherein the load adjustor section comprises a load element group that  
25 includes a plurality of load elements, and a selector section that selects predetermined at least one of the load elements as the first load from the load element group by the selected address.
- 30 5. A semiconductor memory device according to claim 4 further

comprising a common-line path that connects between a plurality of the memory cells and a common terminal, wherein the load element group has load distribution that is equivalent with the common-line path, and the selector section connects each

5 connection point of the load element group corresponding to each connection point of the common-line path to be connected with each of the memory cells is connected to the reference cell.

6. A semiconductor memory device according to claim 5, wherein  
10 the load element group is constituted by a wiring material having physical parameter equivalent with the common-line path in form of wiring geometry equivalent with the common-line path.

7. A semiconductor memory device according to claim 5, wherein  
15 impedance from a connection point of the common-line path to the common terminal is equivalent to impedance from a connection point of the load element group to the common terminal.

8. A semiconductor memory device according to claim 5, wherein  
20 the common terminal is a reference voltage terminal, and source terminal of the reference cell and source terminals of a plurality of the memory cells are connected to each connection point of the load element group and the common-line path.

25 9. A semiconductor memory device according to claim 4 further comprising a common-line path both ends of which are connected to a common terminal, the common-line path connecting with an exponential multiplier of 2 of the memory cells with constant interval taken,

30 wherein the load element groups comprises: a first load

element group in which predetermined number of second load elements are connected in series, the predetermined number of the second load elements being obtained by adding up first load elements arranged between adjoining point on the common-line path to which the memory cells are connected by exponential multiplier of 2; and a second load element group obtained by subtracting the second load element which is largest load from the first load element group, and

the selector section exclusively selects some of the second load elements that mutually correspond to each other between the first load element group and the second load element group.

10. A semiconductor memory device according to claim 1 further comprising:

a first digit line to which a plurality of the memory cells are connected;

a second digit line to which a plurality of the memory cells are connected;

a first data line to which some of the memory cells not to be selected are connected through the first digit line;

a second data line to which one of the memory cell to be selected is connected through the second digit line;

a first loader section that comprises the reference cell and the load adjustor section, and is connected to the first data line; and

a second loader section that has equivalent constitution as the first loader section, and is connected to the second data line;

wherein readout operation is conducted using the first data line and the second data line as a pair.

11. A semiconductor memory device according to claim 1 further comprising:

a first digit line to which a plurality of the memory cells are connected;

5 a second digit line to which a plurality of the memory cells are connected;

a first data line to which some of the memory cells not to be selected are connected through the first digit line;

10 a second data line to which one of the memory cells to be selected is connected through the second digit line;

a first loader section that is connected to the first data line and supplies the reference value to the first data line;

15 a second loader section that has equivalent constitution as the first loader section, and is connected to the second data line; and

a regulator section that comprises the reference cell and the load adjustor section and outputs regulate voltage in accordance with the reference value;

20 wherein the first loader section and the second loader section comprises a first load section and a second load section, respectively, that are controlled by the regulate voltage.

12. A semiconductor memory device according to claim 1 further comprising a plurality of readout operation modes, wherein

25 predetermined readout operation modes among a plurality of the readout operation modes comprises the reference cell and the load adjustor section.

13. A semiconductor memory device according to claim 12,

30 wherein, in case number of the predetermined readout operation

modes is two or more, the load adjustor section is shared among the predetermined readout operation modes.

14. A semiconductor memory device according to claim 12,  
5 wherein, in case number of the predetermined readout operation modes is three or more, a first readout operation modes comprises a first load adjustor section, and other readout operation modes comprise a second load adjustor section modes that is shared among the other readout operation modes.

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15. A semiconductor memory device according to claim 12, wherein the semiconductor memory device is a non-volatile semiconductor memory device, and the predetermined readout operation mode is a data readout mode or at least one of readout operation modes out  
15 following two combinations, namely, the data readout mode and a program-verify mode or the data readout mode and a delete-verify mode.

16. A semiconductor memory device according to claim 1, wherein  
20 the semiconductor memory device is a non-volatile semiconductor memory device, and the reference value is a reference current value.

17. A control method of a semiconductor memory device comprising  
25 the steps of:

    a step for reading out data from a memory cell, and  
    a step for differentially amplifying the data read out from the memory cell with reference to a reference value read out from a reference cell;

30 wherein the reference value is adjusted by adjusting a first

load connected to the reference cell with reference to a second load on a data path of the memory cell selected by a selected address.

- 5 18. A control method of a semiconductor memory device according to claim 17, wherein the first load is equivalent with the second load.